



UNITED STATES PATENT AND TRADEMARK OFFICE

126

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,827	03/23/2004	Yoji Nagase	1324.70101	4226

7590 10/31/2007
Patrick G. Burns, Esq.
GREER, BURNS & CRAIN, LTD.
Suite 2500
300 South Wacker Dr.
Chicago, IL 60606

EXAMINER

HAILEMARIAM, EMMANUEL

ART UNIT	PAPER NUMBER
----------	--------------

2629

MAIL DATE	DELIVERY MODE
-----------	---------------

10/31/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/806,827

Applicant(s)

NAGASE, YOJI

Examiner

Emmanuel Hailemariam

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 08 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>09/13/07</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1,2,5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (figs. 25-28) in view of Shimomaki (7,221,344).

As to Claim 1, Applicant Admitted Prior Art (figs. 25-28) (hereinafter AAPA) discloses a method of driving an active matrix type liquid crystal display panel, **during horizontal scanning periods (fig.27 (scanning periods))**, using a data signal **whose polarity is inverted at the beginning and end of each horizontal scanning period (fig.27 (horizontal scanning period))**, **the driving method also using gate signal (fig.26-28) (12), which is raised and broken down at spaced intervals (fig.27 (gate signal (12))), a selected horizontal scanning period occurring at least in part while the gate signal is raised (fig. 27 (gate signal and horizontal scanning))** comprising the step of: performing a pre-scanning (see figs 27 (pre-scanning)) and a main scanning ((see fig. 27 (main scanning)) to each horizontal line using the gate signal (fig.27 (gate signal) (12)); Applicant Admitted Prior Art (figs 26,27) does not teach "the gate signal is raised in the Main scanning at timing on or after a first inversion of the

data signal occurring during The selected horizontal scanning period and the gate signal is broken down in the main scanning at a timing prior to the next following inversion of the data signal occurring the Horizontal scanning period".

However, the patent of Shimomaki is cited to teach that it is well known for Display driving method to have the gate signal (fig. 9 (VG)) is raised in the main scanning at a timing on or after a first inversion of the data signal (fig.9 (Vsig)) occurring during the selected horizontal scanning period (fig.9 (n-th FIELD)) and the gate signal (fig.9 (Vg)) is broken down in the main scanning at a timing prior to the next following inversion of the data signal occurring the horizontal scanning period (see, fig.9 (Vsig)).

Therefore it would have been obvious to one skill in the art at the time of the invention was made to have incorporate Shimomaki driving method into Applicant's Admitted Prior Art system because this will restrict the deterioration of the display Display device (see, col.3 lines 51-52).

As to claim 2, AAPA discloses a method of driving a liquid crystal display panel according to the timing for raising the gate signal (12) relative to pre-scanning **inverting the polarity of** data signal (10) in the is the same as the timing for raising the gate signal relative to the data signal in the main scanning (see fig 26-28).

As to claim 5, AAPA discloses a method of driving an active matrix type liquid crystal display panel **using a data signal whose polarity is inverted for every horizontal scanning period** (fig.26 (A)), comprising the step of performing a pre-scanning and a main scanning to each horizontal line ((see figs.26-28 (main scan) **the horizontal scanning period has a pre-writing data voltage period where the pre-**

scanning is (B) performed and the main scanning (A) is not performed and another period where the scanning is performed, and a value of a predetermined pre-writing data voltage that is a data voltage period is different from a value of a display data voltage that is a data voltage in said another period (fig.27) (one horizontal scanning period)... period , and a data voltage in the pre-writing data voltage period is used as a predetermined pre-writing data voltage (see fig 27).

As to claim 6 AAPA discloses a method of driving a liquid crystal display panel according to the predetermined pre-writing data voltage is the one of an intermediate gray scale [0019](see fig.26 and 27).

As to claim 7, AAPA discloses a method of driving a liquid crystal display panel according to claim 5, wherein the predetermined pre-writing data voltage is the one between a white voltage and a black voltage of the same polarity as the polarity of the data signals in the main scanning [0019] (see, fig (26,28).

As to claim 8, AAPA discloses a method of driving a liquid crystal display panel according to claim 5, wherein the predetermined pre-writing data voltage is an average gray scale voltage in a frame period for pixels (it is implicit that for LCD to have pixels on it, since each pixels is a point in a graphic image) along the data line [0019] (see fig. 26,27center of data signal).

As to claim 9, AAPA discloses a method of driving a liquid crystal display panel according to claim 5, wherein the predetermined pre-writing data voltage is the one during a main scanning period when the pre-scanning (see figs 26-28(pre-scan) is just preceding the main scanning ((see figs.26-28 (pre scan).

As to claim 10, APPA discloses a method of driving a liquid crystal display panel according to claim 5, wherein the pre-writing data voltage is a voltage that is corrected by an amount of change in a pixel voltage stemming from the break-down of the gate signal at the end of the pre-scanning (see figs 26-28).

As to claim 11, AAPA discloses a method of driving an active matrix type liquid crystal display panel, comprising the step of: performing a pre-scanning (see figs 26-28(pre-scan) and a main scanning to each horizontal line);((see figs.26-28 (main scan); wherein a **value** of gate-off (see.fig.25) voltage between the pre-scanning period and the main scanning period is set to be higher than value the gate-off (see fig.25) voltage after the main scanning period ((see figs.26-28 (main scanning)).

As to claim 12, AAPA discloses an active matrix type liquid crystal display panel comprising a drive circuit driven by a method of driving a liquid crystal display panel [0005].

Claims 3 & 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (Fig.25-28) in view of Yasukatsu et al (JP Pub. Num. 09-274170), (hereinafter referred to as Yasukatsu).

As to claims 3 and 4, AAPA discloses a method of driving an active matrix type liquid crystal display panel, comprising the step of: performing a pre-scanning (see fig. 27 (pre-scanning) and a main scanning to each horizontal line (see fig.27 (main scanning)); an on-voltage of a gate signal in the pre-scanning is different from a **value** an on-voltage (see fig.27).

AAPA does not teach, a length **between timing of raising of gate signal and timing of next following breaking down of the gate signal** ... the pre-scanning period different from the main scanning period.

Yasukatsu, on the other hand, teaches a method wherein a length of the pre-scanning period (Yasukatsu teaches the length of the preparatory write-period is contained in the 1st half of the selection period) is different from a length of the main scanning period (Yasukatsu teaches the length of the write-in period is half of the second half of the selection period). (See Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify AAPA method by making the length of the pre-scanning period different from a length of the main scanning period. The motivation to have different lengths of period for pre-scanning and scanning is to prevent the over-heating of the LCD as stated by Yasukatsu in the abstract.

Response to Arguments

3. Applicant's arguments with respect to claim 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2629

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contacts

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Hailemariam whose telephone number is 571-270-1545. The examiner can normally be reached on M-F 8:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2629

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emmanuel Hailemariam

09/23/07



AMARE MENGISTU
SUPERVISORY PATENT EXAMINER